IN THE CLAIMS

Please amend claim 11 as hereinbelow.

1. (Original) A high frequency power amplifier circuit which comprises two or more cascaded field effect transistors for amplification and controls output power by controlling power voltages of the field effect transistors for amplification to gate terminals of which bias voltages of a predetermined level are applied,

wherein different transistors for power voltage control are provided for a last-stage field effect transistor for amplification and preceding-stage field effect transistors for amplification, and a power voltage is generated and applied by the transistors for power voltage control so that the preceding-stage field effect transistors for amplification have drain currents saturated in a state of a lower control voltage than the last-stage field effect transistor for amplification.

2. (Original) The high frequency power amplifier circuit according to claim 1,

wherein control terminals of the transistors for power voltage control are applied with output voltages of differential amplifier circuits to which two voltages are inputted, one voltage being a control voltage for controlling output power of the high frequency power amplifier circuit, and the other voltage being voltage supplied to at least a transistor for amplification of a last stage of the high frequency power amplifier circuit from the transistors for power voltage control.

3. (Original) The high frequency power amplifier circuit according to claim 1,

wherein a control voltage for controlling output power of the high frequency power amplifier circuit is inputted to the control terminals of the transistors for power voltage control.

4. (Original) A high frequency power amplifier circuit which comprises two or more cascaded field effect transistors for amplification and controls output power by controlling power voltages of the field effect transistors for amplification to gate terminals of which bias voltages of a predetermined level are applied,

wherein a transistor for power voltage control is provided on a drain side of a last-stage field effect transistor for amplification, preceding-stage field effect transistors for amplification are configured by a dual-gate field effect transistor, an

output control voltage is applied to a gate terminal of the transistor for power voltage control and one gate terminal of the dual-gate field effect transistor so that drain voltages of the field effect transistors for amplification of the different stages can be controlled independently, and the preceding-stage field effect transistors for amplification have drain currents saturated in a state of a lower control voltage than the last-stage field effect transistor for amplification.

5. (Original) A high frequency power amplifier circuit which comprises two or more cascaded field effect transistors for amplification and controls output power by controlling power voltages of the field effect transistors for amplification to gate terminals of which bias voltages of a predetermined level are applied,

wherein a transistor for power voltage control is provided on a drain side of a last-stage field effect transistor for amplification, preceding-stage field effect transistors for amplification are connected in series, with second field effect transistors, an output control voltage is applied to a gate terminal of the transistor for power voltage control and each of gate terminals of the second field effect transistors so that drain voltages of the field effect transistors for amplification of the different stages can be controlled independently, and the preceding-stage field effect transistors for amplification have drain currents saturated in a state of a lower control voltage than the last-stage field effect transistor for amplification.

6. (Original) The high frequency power amplifier circuit according to claim 4,

wherein the output control voltage is directly applied to one gate terminal of the dual-gate field effect transistor.

7. (Original) The high frequency power amplifier circuit according to claim 5,

wherein the output control voltage is directly applied to gate terminals of the second field effect transistors.

8. (Original) The high frequency power amplifier circuit according to claim 4,

wherein control terminals of the transistors for power voltage control are applied with output voltages of differential amplifier circuits to which two voltages are inputted, one voltage being a control voltage for controlling output power of the

high frequency power amplifier circuit, and the other voltage being voltage supplied to at least a transistor for amplification of a last stage of the high frequency power amplifier circuit from the transistors for power voltage control.

9. (Original) The high frequency power amplifier circuit according to claim 1,

wherein the transistors for amplification are formed so that an element size of the preceding-stage transistors for amplification is larger than an element size of the last-stage transistor for amplification.

10. (Original) The high frequency power amplifier circuit according to claim 1,

wherein the bias voltage applied to the gate terminals of the transistors for amplification is set so that a voltage applied to the gate terminals of the preceding-stage transistors for amplification is lower than a voltage applied to the gate terminal of the last-stage transistor.

11. (Currently Amended) A radio communication system comprising: the high frequency power amplifier circuit ~~according to claim 1~~ which comprises two or more cascaded field effect transistors for amplification and controls output power by controlling power voltages of the field effect transistors for amplification to gate terminals of which bias voltages of a predetermined level are applied, wherein different transistors for power voltage control are provided for a last-stage field effect transistor for amplification and preceding-stage field effect transistors for amplification, and a power voltage is generated and applied by the transistors for power voltage control so that the preceding-stage field effect transistors for amplification have drain currents saturated in a state of a lower control voltage than the last-stage field effect transistor for amplification; a baseband circuit that converts an audio signal into a baseband signal and converts a received signal into an audio signal; and a modulation/demodulation circuit that demodulates the received signal and modulates a transmission signal,

wherein the high frequency power amplifier circuit amplifies and outputs a transmission signal modulated by the modulation/demodulation circuit according to an output control voltage supplied from the baseband circuit or the modulation/demodulation circuit to the high frequency power amplifier circuit.

12. (Original) The radio communication system according to claim 11, including a first high frequency power amplifier circuit for amplifying signals of a first frequency band and a second high frequency power amplifier circuit for amplifying signals of a second frequency band,

wherein the transistor for power voltage control is provided as a circuit common to the first high frequency power amplifier circuit and the second high frequency power amplifier circuit, and different power voltages are generated in accordance with signals to be transmitted.